REMARKS

This is intended as a full and complete response to the Office Action dated July 25, 2005, having a shortened statutory period for response set to expire on October 25, 2005. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-19 are pending in the application. Claims 1-19 remain pending following entry of this response. Claims 1 and 17 have been amended. Applicant submits that the amendments do not introduce new matter.

Claim Rejections - 35 USC § 102

Claims 1-4, 6, 7, 10-14, 16, 17 and 18 are rejected under 35 U.S.C. 102(a) as being anticipated by *Tsubouchi et al.* (US 2002/0186609 A1, hereinafter "*Tsubouchi*").

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). In this case, *Tsubouchi* does not disclose "each and every element as set forth in the claim", as described below.

With respect to claim 1, and the claims that depend therefrom, the claims describe, during read-out of a memory cell, activating a word line and amplifying, with a sense amplifier, a charge difference brought about thereby on the bit lines to generate a high charge potential and a low charge potential. During refresh of the memory cell, the word line is activated and the charge potentials of the bit lines are amplified with the sense amplifier, depending on charge information of the memory cell, in the direction of a high refresh potential and a low refresh potential. After the refresh, the potentials of the bit lines are charged to a second center potential. The potential difference between the high refresh potential to which the sense amplifier drives the bit lines during refresh and the second center potential is greater than the potential difference between the high

charge potential to which the sense amplifier drives the bit lines during readout and a first center potential.

This claimed relationship between the high potentials and center potentials may be created, for example, by making the high refresh potential greater than the high charge potential (see, for example, claim 2) or by making the first center potential greater than the second potential (see, for example, claim 5). As an example of making the high refresh potential greater than the high charge potential, the specification describes a control circuit used to apply a first high potential and a second high potential to a sense amplifier. See Para. [0038]; Fig. 1, Items 6, 9, 10, 4. When the sense amplifier is used to amplify a charge difference stored in a memory cell, a changeover switch selects between the first and second potentials depending on whether a read/write or a refresh is being performed. See Paras. [0043]-[0044]; Fig. 1, Item 9, 10, 11, 13. As an example of making the first center potential greater than the second center potential, the specification describes that one of two center potentials may be selected via a change switch and applied by equalization transistors to the bit lines depending on whether a read/write or a refresh is being performed. See Paras. [0057]-[0058]; Fig. 5, Items 15, 16, 17, 14.

The Examiner states that *Tsubouchi* discloses "after the refresh, charging the potentials of the bit lines to a second center potential, wherein the potential difference between the high refresh potential and the second center potential is greater than the potential difference between the high charge potential and the first center potential" at Para. [0148]. However, the cited passage is in fact directed to potential differences ($\Delta V0$ and $\Delta V1$) generated by a memory cell and not a potential difference between a high refresh potential and a second center potential which is greater than a potential difference between a high charge potential and a first center potential as claimed.

The cited section describes a potential difference $\Delta V1$ that is read during a refresh operation which becomes greater than a potential difference $\Delta V0$ that is read during a normal operation. *See* Para. [0148]. $\Delta V0$ and $\Delta V1$ are generated by a memory cell between bitlines BL and ZBL. *See* Paras. [0148] and [0037]. To equalize the potential of bitline BL and ZBL, an equalize circuit BEQ supplies VBL to BL and ZBL when an equalize signal BLEQ is received. *See* Paras. [0128]-[0129]; Figs. 6 and 9.

As clearly depicted in Figs. 6 and 9, the difference between the voltage applied by the sense amp SAK during a sense operation (VCC – the ground voltage) while amplifying ΔV0 or ΔV1 and the voltage applied by the equalize circuit BEQ during an equalize operation (VBL) remains constant (VCC – the ground voltage - VBL), and is not varied depending on whether a refresh or a read operation is being performed. *See* Paras [0128]-[0132]; Figs. 6 and 9. Accordingly, *Tsubouchi* does not describe "after the refresh, charging the potentials of the bit lines to a second center potential, wherein the potential difference between the high refresh potential to which the sense amplifier drives the bit lines during refresh and the second center potential is greater than the potential difference between the high charge potential to which the sense amplifier drives the bit lines during readout and the first center potential". Withdrawal of the rejection is respectfully requested.

With respect to claim 10, and the claims that depend therefrom, the claims describe a voltage control means for varying the potential difference between the high charge potential and the common center potential, wherein the potential difference between the high charge potential and the common center potential during a refresh of the memory cell is greater than the potential difference between the high charge potential and the common center potential during a read-out of the memory cell. As described above, the voltage applied by the sense amp SAK during a sense operation while amplifying ΔV0 or ΔV1 and the voltage applied by the equalize circuit BEQ during an equalize operation remains constant whether a refresh or read of a memory cell is being performed. *See* Paras [0128]-[0132]; Figs. 6 and 9. Accordingly, Applicant submits that *Tsubouchi* does not teach the claimed voltage control means. Withdrawal of the rejection is respectfully requested.

With respect to claim 17, and the claims that depend therefrom, the claims describe first and second potential sources, wherein the first potential source is greater than the second potential source and a voltage control circuit configured to provide the sense amplifier with the high charge potential from the first potential source during refresh of the memory cell and from a second high potential source during read-out of the memory cell. As described above, the sense amplifier SAK described in *Tsubouchi* only applies a single potential (VCC – the ground voltage) during a refresh or a read

operation, regardless of which respective operation is being performed. *See* Paras [0128]-[0132]; Figs. 6 and 9. Accordingly, Applicant respectfully submits that *Tsubouchi* does not teach the claimed limitations. Withdrawal of the rejection is respectfully requested.

Therefore, each of the claims are believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Allowable Subject Matter

Claims 5, 8, 9, 15 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant acknowledges the allowable subject matter but respectfully submits that the rejection of the base claims has been overcome for the reasons stated above. Allowance of the claims is respectfully requested.

Conclusion

The secondary references made of record are noted. However, it is believed that the secondary references are no more pertinent to the Applicant's disclosure than the primary references cited in the office action. Therefore, Applicant believes that a detailed discussion of the secondary references is not necessary for a full and complete response to this office action.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,

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